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transforming a portion of said conductive layer adjacent said insulator element region into a sidewall spacer after forming the insulator element region.

REMARKS

Rejections under Double Patenting

The Examiner has rejected Claims 1-15 and 23-28 under the judicially created doctrine of obviousness-type double patenting as being unpatentable over Claims 1-8 of U.S. Patent No. 5,405,791. Applicant respectfully traverses the rejections and submits that the pending claims in the present application are patentably distinct from the claims of U.S. Patent No. 5,405,791 ("Ahmad").

The claims of the Ahmad patent reflect the disclosure of Ahmad, which is distinguished below. In particular, the claims of Ahmad relate to forming disposable spacers, by deposition, and implanting ***conductivity-enhancing dopants***, not to "transforming" a portion of the gate conductor, nor to implanting "insulator elements" in the substrate.

Rejections under 35 U.S.C. § 103(a)

The Examiner has rejected Claims 1-15 and 23-28 under 35 U.S.C. § 103(a) as being unpatentable over Ahmad et al. (U.S. Patent No. 5,405,791) in view of Wu et al. (U.S. Patent No. 5,837,585).

Applicant's independent Claim 1 recites forming an insulator element region on the substrate and ***transforming*** a portion of the conductive layer adjacent said insulator element region into a sidewall spacer ***after*** forming the insulator element region. Furthermore, Applicant has amended Claim 1 to recite forming the insulator element ***directly*** on the substrate.

The Examiner asserts that Ahmad taught forming an insulator element region on the substrate and forming a sidewall spacer.

Referring to Figure 2 in Ahmad, a conventional source/drain reoxidation step formed a thermal oxide layer 21 on the surface of the source/drain regions and on the sidewalls of both N-channel and P-channel transistor gates (Col. 3, lines 54-57). A slilicon nitride etch stop layer 24 is deposited ***after*** the source/drain reoxidation (Col. 3, lines 63-65). Thus, under any interpretation, Ahmad taught transforming a portion of the conductive layer into a sidewall spacer ***at the same time as or before*** forming an insulator element region, not after forming an insulator element region as Applicant has recited.

In the process of Ahmad, several subsequent steps involve chemical vapor deposition of TEOS followed by a spacer etch. But Ahmad contained no teachings about ***transforming*** a conductive layer into a spacer ***after*** forming an insulator element region. Furthermore, Ahmad taught forming the etch stop layer 24 over the grown oxide 21, in contrast to Applicant's amended Claim 1, which recites forming an insulator element directly on the substrate.

In order to supply the deficiencies of Ahmad, the Examiner offers Wu as a reference for teachings about nitrogen implantation, to meet the limitations of Claim 13 ("implanting an ***insulator element***") and Claim 15 ("implanting nitrogen"), as examples.

With respect to Claim 1, Wu did not teach or suggest transforming a conductive layer into a spacer after forming an insulator element region. Furthermore, the Examiner has offered no additional reference to combine with Ahmad to show obviousness for Applicant's recitations in Claim 1.

Accordingly, Applicants respectfully submit that independent Claim 1 is allowable over the art of record.

Independent Claims 13, 15 and 23 contain recitations about implanting an insulator element, implanting nitrogen and forming a nitrogen doped region, respectively. The Examiner asserts that "it would have been obvious to one of ordinary skill in the art at the time of the invention to substitute Ahmad's arsenic with Wu's nitrogen in Ahmad's process to form an oxide layer with very high electron injection efficiency and a very large charge-to-breakdown voltage." (Paper 6, page 4) The Examiner states this as the basis for rejection of pending .?

Ahmad taught "a boron halo implant which creates N-channel anti-punchthrough regions 61, and low dosage arsenic source/drain implant which creates lightly-doped N-channel source/drain regions 62." (Col. 4, ln. 29-33) The skilled artisan would understand that the purpose of these dopings was to tailor the conductivity of transistor structures.

Wu taught nitrogen to nitridize a thin tunnel oxide, and thus improved the flash memory cell formed therefrom.

Accordingly, the skilled artisan would not have been motivated to employ the nitrogen implantation of Wu, whose purpose was to increase performance of flash memory cell tunnel oxides, for the arsenic and boron doping of Ahmad, whose purpose was to increase conductivity of transistor structures in the substrate. There is no suggestion or motivation to combine these references. Whereas arsenic and boron increase the conductivity of silicon, nitrogen makes silicon

less conductive. In fact, using the nitrogen implantation of Wu in place of arsenic and boron in the transistor of Ahmad would render Ahmad inoperative.

Applicants respectfully traverse the rejections insofar as they apply to independent Claims 1, 13, 15 and 23 and submit that the pending claims are patentably distinct.

Dependent Claims 2-12, 14 and 24-28 each depend from one of these independent claims and therefore include all the features and limitations thereof. Furthermore, the dependent claims add further distinguishing features of particular utility. Accordingly, Applicants submit that the dependent claims are also allowable over the art of record.

CONCLUSIONS

In view of the foregoing remarks, Applicant respectfully requests reconsideration of the claims and submits that the application is in condition for allowance. If, however, some issue remains which the Examiner feels may be addressed by Examiner's amendment, the Examiner is cordially invited to call the undersigned for authorization.

Respectfully submitted,
KNOBBE, MARTENS, OLSON & BEAR, LLP

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

1. (Twice Amended) A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

forming an insulator element region directly on said substrate; and

transforming a portion of said conductive layer adjacent said insulator element region into a sidewall spacer after forming the insulator element region.